LOW TEMPERATURE EPITAXIAL GROWTH OF SI AND SIGE AND THEIR TRANSFER TO FOREIGN SUBSTRATE

R. Cariou[a,b,*], I. Massiot[c], R. Ruggeri[d], N. Ramay[a], J. Tang[a,e], A. Cattoni[c], S. Collin[c], J. Nassar[a] and P. Roca i Cabarrocas[a]

[a]LPICM, CNRS, Ecole Polytechnique, 91128 Palaiseau, France
[b]III-V lab, joint laboratory between Alcatel-Lucent Bell Labs France, Thales Research and Technology and CEA-LETI, route de Nozay, 91460 Marcoussis, France
[c]Laboratoire de Photonique et de Nanostructures, CNRS, Route de Nozay, 91460 Marcoussis, France
[d]Dipartimento di Fisica della Materia e Ingegneria Elettronica, Università di Messina, Salita Sperone 31, 98166 Messina, Italy
[e]ICARE - China-Europe Institute for Clean and Renewable Energy at Huazhong University of Science and Technology, 1037 Luoyu road, Wuhan, PR China 430074

Using a standard RF-PECVD reactor, silicon layers are epitaxially grown at 175°C. Few µm thick layers can be efficiently used as an absorber in the wafer equivalent approach: p++c-Si(wafer) / epi-Si(~µm) / n+aSi:H(12nm) has excellent diodes characteristics with FF of 80.5 % and 8,8% efficiency. By dilution of GeH_4 in SiH_4/H_2 plasma, we show for the first time epitaxial SiGe alloys, with variable Ge fraction, grown at such low temperature. Structural and electronic properties of these materials has well has solar cells parameters are investigated using spectroscopic ellipsometry, Raman, TEM, J(V) characteristics and EQE. Using stress induced lift off technique ultra-thin Si layers of few cm^2 are transferred on inexpensive substrates. Material quality is kept constant during the transfer process as shown by Raman FWHM of 5.3 cm^{-1}, and ultra-thin heterojunctions solar cells are processed on foreign substrates. Preliminary results suggest lifetimes in higher than 67 µs for passivated 3,2µm thick transferred epitaxial PECVD grown layers.

Keywords: Epitaxy, PECVD, Thin Film Solar Cell, Flexible substrate

1 INTRODUCTION

Nowadays, the large majority of photovoltaic modules are based on crystalline silicon wafers. Huge progress were made for silicon solar cells since the first patented PN junction [1]. Indeed, the learning curve for c-Si has reached a plateau since 1999 with the 25% efficiency cell with passivated emitter rear locally diffused (PERL) architecture, developed by M. Green et al. [2]. Recently, the so-called heterojunction with intrinsic thin layer (HIT) concept, with amorphous silicon for c-Si wafer passivation and junction formation, is getting closer to the same limit, with a 24.7% on large area, reported by Panasonic [3]. Still, the highly purified silicon material remains a main component of the module cost; thus industry has constantly kept decreasing the wafer thickness down to 150 µm today. However, sawing and breakage losses are a serious issue for going thinner and no technological solutions exist yet for such thickness. The thin film solar cells (a-Si:H, CdTe, CuIn(Ga)Se, etc.) aim to tackle this problem: despite average lower efficiency than c-Si they involve nevertheless low cost processes and low material consumption. Yet, some of these technologies have a hidden cost, that is the scarcity, or even the toxicity of the materials they rely on, and that will limit their development on the longer term and large scale. In contrast, thin films of *crystalline* silicon, combined with good light trapping, would solve the issues of c-Si wafer thickness limitation, limited stability and efficiency and those of scarcity and toxicity at the same time. Research in this field is now focusing on three axes: i) Production of few µm thin c-Si layers ii) Transfer to low cost substrates iii) Advanced light trapping schemes (plasmonics, photonics, etc.) with efficient schemes to compensate for light absorption losses in ultra-thin layers.

2 INNOVATIVE LOW TEMPERATURE RF-PECVD EPITAXY APPROACH

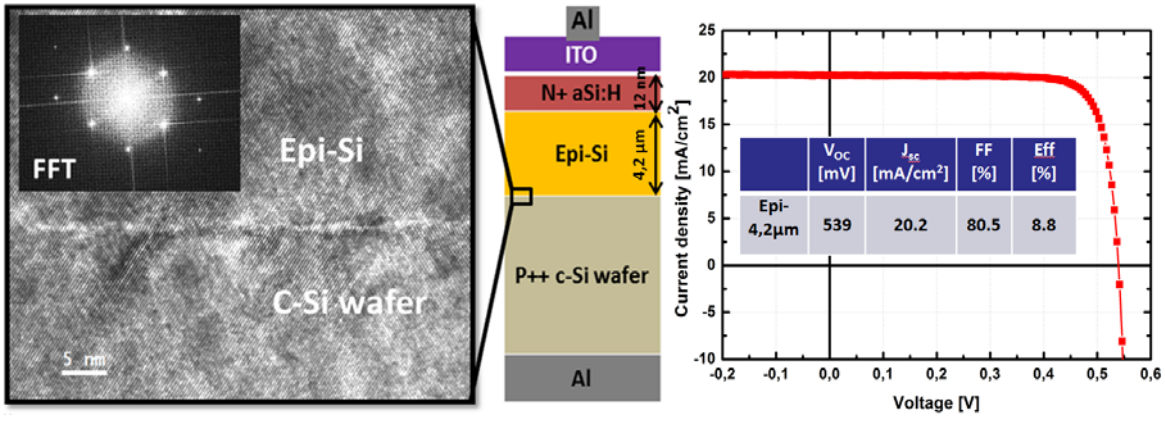

Figure 1: Left cross section TEM image of wafer/epi-Si interface. Right: current-voltage curve of 4,2 µm thick epi-Si absorber cell; Solar cell structure shown in the middle.

The top down approach, i.e. exfoliation or wafer etching, has shown promising results such as 21.5 % efficiency for 47 µm cell, or recently 4.8 % for much thinner cell: 1 µm epi-free c-Si cell [4–6]. Bottom up approach of epitaxy on inexpensive crystal seed and/or layer transfer can further reduce cost through growth substrate reuse. Many groups are working in that direction [7–11], and this epitaxial technology is already matching wafer based efficiency, according to the 20.1% - 43 µm thick reported in 2012 by Solexel company. Within this context, we have developed a RF-PECVD epitaxial process that enables the growth of mono-crystalline Si and Ge layers [12,13] at very low temperature [150-200°C]. For the first time, we report here SiGe alloys epitaxial growth at such low temperature; they are used as an absorber in wafer equivalent solar cells. The combination of epitaxy with standard RF-PECVD deposition tool and stress induced lift off [14] is used to produced ultra-thin epitaixal foils on inexpensive substrate. Moreover, transferred crystalline Si based layers enable to access and study properly fundamental parameters such as life time and passivation.

3 THIN EPITAXIAL SOLAR CELLS

Epitaxial layers are grown on (100) oriented c-Si wafer cleaned by HF dipping. Following the chemical cleaning, p++ c-Si ($\rho=10^{-3}$ Ω.cm) substrates are loaded inside standard 13.56 MHz RF-PECVD reactor and pumped down to 10^{-7} mbar within 45 min (no load-lock). Deposition is done at 175 °C from SiH_4, GeH_4 and H_2 gas precursors. This specific growth process occurs at a pressure of 2 Torr, most probably from plasma synthetized nano-clusters that melt by impacting the surface, enabling subsequent epitaxial growth [15,16]. A thin n-type amorphous layer is then deposited to form the junction in the same reactor (see cell scheme on Fig. 1)). Structural properties of PECVD grown layers are wafer/epi-Si interface is shown on left part of figure Fig. 1). Mono-crystal quality is confirmed by FFT, and interface layer, also detected by ellipsometry, is visible. This non-perfect interface, mostly due to cleaning procedure and air exposure before loading substrate into reactor, has fragile mechanical properties that may enable easy lift off. Epitaxial layers have high hydrogen content (0,1% by SIMS), incorporated during the low growth temperature, which provide a positive effect of defect self-passivation. J-V curve of the wafer equivalent structure is shown, on Fig.1). p++c-Si(wafer) / epi-Si(4,2µm) / n+aSi:H (12nm) can achieve the noteworthy 8.8 % efficiency, short circuit current of 20.2 $mA.cm^{-2}$ and fill factor of 80.5%. Such high FF is the proof of high quality material; however open circuit voltage of 534 mV remains lower than the expected values. This is attributed to the defect-rich interface layer, and lift off solar cells is allowing significant improvement in that direction.

4 ABSORPTION ENHANCEMENT AND LIFT-OFF

Aiming at increasing current in crystalline layers of few microns, we have explored the possibility of epitaxial growing SiGe by PECVD. Fig. 2) shows imaginary part of pseudo-dielectric function of PECVD epitaxial layers as well as the reference curves for c-Si (black line) and c-Ge (bright green line). Epitaxial layers are perfectly fitting by 100 % mono-crystalline material, with ~1 nm porous interface with the substrate**.** The **s**mall discrepancy, for 4.2 eV peak, between pure epitaxial silicon (red dots) and theoretical c-Si is explained by roughness and oxide presence on epi-layer surface while oscillations at low energy part of the spectrum is linked to the small defective layer at interface. By controlling the germane dilution in plasma gas precursor, epi-SiGe layers are grown with variable Ge fraction (see colored dots on Fig. 2)), with Ge% up to 35%. Performances of epitaxial solar cells with pure silicon and SiGe (27% Ge), both 1,8µm thick absorber, were compared. Results (not shown here) is more than 1 mA/cm^2 increase in current; however Voc is decreased down to 440 mV, which is due to band gap reduction and defects arising from c-Si/SiGe interface. Futur implementation of graded SiGe buffer layer should help to improve this aspect.

Stress induced by PECVD grown layers lift-off and transfer is done with the following process: Fig. 2): a) Metal evaporation (e.g. Al,Cr) is done on cleaned epi-

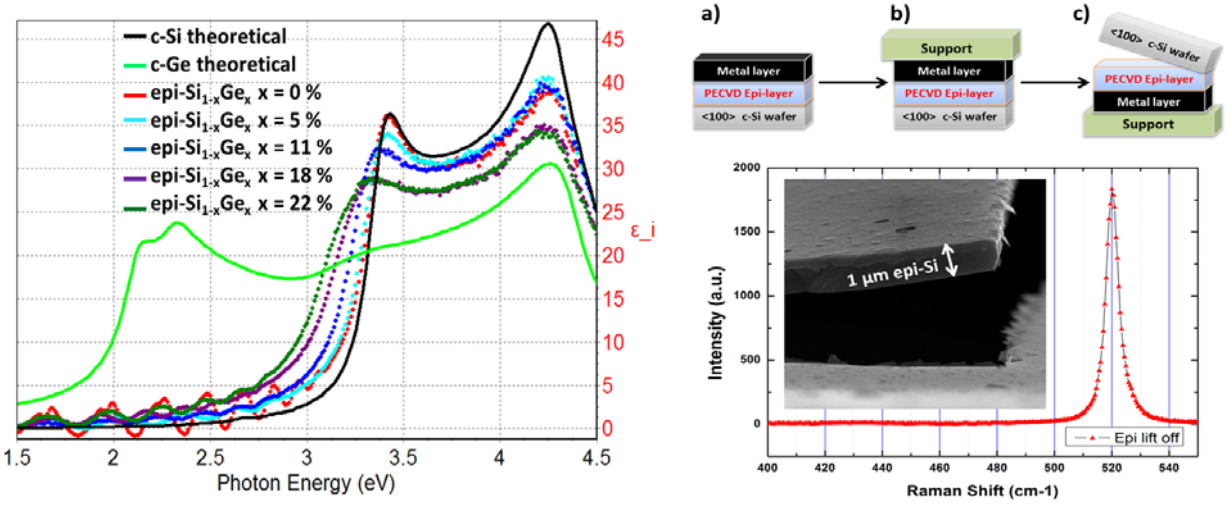

Figure 2: Left: Imaginary part of pseudo-dielectric function of c-Si and c-Ge materials, together with PECVD epitaxially grown SiGe with variable Ge content. Right: stress induced epitaxial layer lift off process: a) PECVD epitaxy and metal evaporation, b) sample attached to handling layer c) rapid thermal annealing for lift off: break occurs at epi-Si/wafer fragile interface. Well defined Raman pic of 1µm thick free standing epi-Si layer, as shown on SEM picture

layer surface, b) Handling substrate (e.g. glass) is glued to the metal surface to allow further processing, b) Few minutes annealing at 400°C under atmospheric pressure. Metal thickness and thermal expansion coefficient plays an important role in this lift off process as well as the fragile layer at epi-Si/wafer interface, where the crack initiate. Layers as thick as 5 µm for few cm^2 are transferred on glass using this method. Constant crystal quality is kept through the process, as shown by the Raman spectrum of 1µm lift off epitaxial Si layer on Fig. 2): peak position is centered on 520.3 cm^{-1} and FWHM is 5.3 cm^{-1}, thus confirming the good quality of lift off mono-crystalline layer. Passivation and lifetime of transferred layer is studied by time resolved microwave conductivity (TRMC). Change is microwave reflectivity related to excess carrier created by 532nm pulsed laser (4ns FWHM) is detected. Diffusion, recombination and laser created carriers are responsible for the evolution of minority carrier concentration. Boundaries conditions at surfaces are imposed by surface recombination velocities. Solution of this problem can be described as an infinite sum of modes with various decay time constant [17,18]. The effective lifetime corresponds to long decay, whereas fast decay modes are related to surface recombination. Measurement on 3,2 µm epi-Si layer, detached from its growth substrate, and a-Si:H passivated is shown on Fig.3. By fitting, we could extract τ_{eff} = 67 µs, which is a lower limit for bulk lifetime of our sample. This value corresponds to a diffusion length exceeding the layer thickness by at least one order of magnitude; this is a proof of excellent electrical properties of the layer.

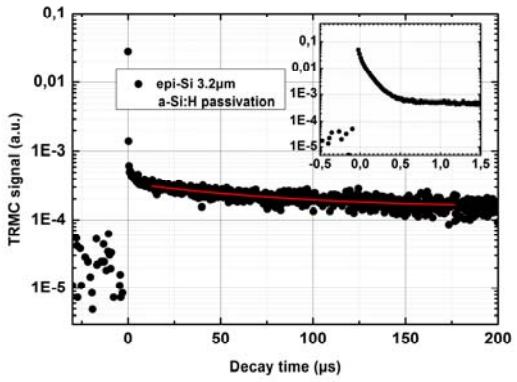

Figure 3: TRMC signal of 3,2 µm detached epi-Si layer passivated by amorphous silicon. Excitation 532nm pulsed laser, and injection level in the range of 10^{16} cm^{-3}.

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REFERENCES

[1] 2402662 (25 June 1946).

[2] M. A. Green, Prog. Photovoltaics Res. Appl. **17**, 183 (2009).

[3] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, Prog. Photovoltaics Res. Appl. **21**, 1 (2013).

[4] A. Wang, J. Zhao, S. R. Wenham, and M. A. Green, Prog. Photovoltaics Res. Appl. **4**, 55 (1996).

[5] R. A. Rao, L. Mathew, S. Saha, S. Smith, D. Sarkar, R. Garcia, R. Stout, A. Gurmu, E. Onyegam, D. Ahn, D. Xu, D. Jawarani, J. Fossum, and S. Banerjee, in *2011 37th IEEE Photovolt. Spec. Conf. PVSC* (2011), pp. 001504 –001507.

[6] C. Trompoukis, O. El Daif, V. Depauw, I. Gordon, and J. Poortmans, Appl. Phys. Lett. **101**, 103901 (2012).

[7] R. B. Bergmann, C. Berge, T. J. Rinke, J. Schmidt, and J. H. Werner, Sol. Energy Mater. Sol. Cells **74**, 213 (2002).

[8] P. Rosenits, F. Kopp, and S. Reber, Thin Solid Films **519**, 3288 (2011).

[9] K. Van Nieuwenhuysen, M. R. Payo, I. Kuzma-Filipek, J. Van Hoeymissen, G. Beaucarne, and J. Poortmans, Thin Solid Films **518**, S80 (2010).

[10] H. M. Branz, C. W. Teplin, M. J. Romero, I. T. Martin, Q. Wang, K. Alberi, D. L. Young, and P. Stradins, Thin Solid Films **519**, 4545 (2011).

[11] J. H. Petermann, D. Zielke, J. Schmidt, F. Haase, E. G. Rojas, and R. Brendel, Prog. Photovoltaics Res. Appl. **20**, 1 (2012).

[12] R. Cariou, M. Labrune, and P. Roca i Cabarrocas, Sol. Energy Mater. Sol. Cells **95**, 2260 (2011).

[13] M. Labrune, X. Bril, G. Patriarche, L. Largeau, O. Mauguin, and P. Roca i Cabarrocas, EPJ Photovoltaics **3**, 30303 (2012).

[14] M. Moreno and P. R. i Cabarrocas, EPJ Photovoltaics **1**, 6 (2010).

[15] N. Ning and H. Vach, J. Phys. Chem. A **114**, 3297 (2010).

[16] P. Roca i Cabarrocas, K. h. Kim, R. Cariou, M. Labrune, E. v. Johnson, M. Moreno, A. T. Rios, S. Abolmasov, and S. Kasouit, MRS Online Proc. Libr. **1426**, 319 (2012).

[17] A. B. Sproul, J. Appl. Phys. **76**, 2851 (1994).

[18] K. L. Luke and L.-J. Cheng, J. Appl. Phys. **61**, 2282 (1987).